EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	20	(predict$3 near3 (clock near1 skew))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/13 16:58
S2	28	((predict$3 or verif$6) near3 (clock near1 skew))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/13 17:31
S3	1821	(clock adj tree or clock-tree with synchron$6)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/13 17:07
S4	223	(clock adj tree or clock-tree) with synchron$6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/13 17:08
S5	40	((clock adj tree or clock-tree) with synchron$6).ab.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/13 17:08
S6	13	S5 and skew.ab.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/13 17:08
S7	0	(incomplete or unfinished) near2 (integrated adj circuit adj2 design)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/13 17:32
S8	57	(incomplete or unfinished) near2 (integrated adj circuit)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/13 17:33

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S9	1	S8 and skew	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/13 17:45
S10	22	simulat$4 same (clock near3 routing)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/14 09:57
S11	232	design near3 (clock adj tree)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/15 14:04
S12	136	S11 and (clock adj skew)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/14 16:10
S13	8	clock adj grid and clock adj skew and partit$5 same clock	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/15 10:49
S14	0	non$planer adj2 clock adj2 tree	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/14 17:53
S15	3	non$planar adj2 clock adj2 tree	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/15 09:06
S16	23	clock adj2 grid same clock adj2 tree	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/15 09:07

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S17	65	distribut$4 adj2 clock adj2 driver	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/15 09:07
S18	0	clock near3 rout$3 near3 different near3 layer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/15 10:49
S19	0	(clock near3 rout$3) same (different near3 layer)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/15 10:50
S20	0	"L11" and largest near2 (clock adj (source or driver))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/15 14:08
S21	0	"L11" and ((largest or biggest) near2 (clock adj (source or driver)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/15 15:03
S22	6	(("5656963") or ("6952117") or ("6934924") or ("6397375") or ("6311313") or ("6006025")).PN.	USPAT; USOCR	OR	OFF	2006/03/15 15:05
S23	6	"447946".ap.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/17 07:55
S24	4	"230197".ap.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/15 15:06

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S25	853	703/13.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/17 07:56
S26	1	S25 and (clock adj2 grid)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/17 07:57
S27	10300	"716".CLAS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/17 07:57
S28	33	S27 and (clock adj2 grid)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/17 07:57
S29	24	S28 and (clock adj skew)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/17 07:57

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IEEE CNF	IEEE Conference Proceeding
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1 Itanium processor clock design

Utpal Desai, Simon Tam, Robert Kim, Ji Zhang, Stefan Rusu

May 2000 **Proceedings of the 2000 international symposium on Physical design**

Publisher: ACM Press

Full text available: pdf(117.47 KB) Additional Information: full citation, references

Keywords: IA-64, Itanium processor, clock distribution, deskew, on-die-clock-shrink

2 Highlights of ISSCC: high-speed heterogenous design techniques: Design of a 10GHz clock distribution network using coupled standing-wave oscillators

Frank O'Mahony, C. Patrick Yue, Mark A. Horowitz, S. Simon Wong

June 2003 **Proceedings of the 40th conference on Design automation**

Publisher: ACM Press

Full text available: pdf(659.48 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, a global clock network that incorporates standing waves and coupled oscillators to distribute a high-frequency clock signal with low skew and low jitter is described. The key design issues involved in generating standing waves on a chip are discussed, including minimizing wire loss within an available technology. A standing-wave oscillator, a distributed oscillator that sustains ideal standing waves on lossy wires, is introduced. A clock grid architecture comprised of coupled, sta ...

Keywords: clock distribution, coupled oscillators, distributed oscillators, on-chip phase measurement, resonant clocking, salphasic, standing wave

3 Process variation: Worst case clock skew under power supply variations

Min Zhao, Kaushik Gala, Vladimir Zolotov, Yuhong Fu, Rajendran Panda, R. Ramkumar, Bhuwan Agrawal

December 2002 **Proceedings of the 8th ACM/IEEE international workshop on Timing issues in the specification and synthesis of digital systems**

Publisher: ACM Press

Full text available: pdf(153.59 KB) Additional Information: full citation, abstract, references, citings, index terms

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